

REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1-20 are pending in the present application.- Claim 3 has been amended.

II. Rejection(s) under 35 U.S.C § 112

Claim 3 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Particularly, the Examiner indicated that there was insufficient antecedent basis for “the range” in claim 3. In response, Applicant has corrected this antecedent basis error by amending claim 3 to be dependent from claim 2, wherein claim 2 recites “a range.” Accordingly, withdrawal of this rejection is respectfully requested.

III. Rejection(s) under 35 U.S.C § 102

U.S. Patent No. 5,629,860

Claims 15-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,629,860 issued to Jones et al. (hereinafter “Jones”). For the reasons set forth below, this rejection is respectfully requested.

The claimed invention is directed toward a method for creating a wire load model

using specific interconnect information. Independent claim 15 requires at least that parasitic information generated for an interconnect configuration be stored in an accessible format, and independent claim 19 requires at least that a wire load model creation tool comprise means for storing the parasitic information. The Examiner asserts that this limitation/feature is disclosed in column 5, lines 7-12 of Jones. However, the reference to writing information in an accessible format refers to information relating to average wire lengths (Jones, column 5, lines 4-7), not parasitic information as required by independent claims 15 and 19 of the present application. Thus, Jones fails to disclose every limitation of these claims. Moreover, Jones altogether is directed to wire lengths whereas the claimed invention relates primarily to wire loads.

In view of the above, Jones fails to show or suggest the present invention as recited in independent claims 15 and 19. Thus, independent claims 15 and 19 are patentable over Jones. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

U.S. Patent No. 5,694,344

Claims 15, 16, and 18 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,694,344 issued to Yip et al. (hereinafter "Yip"). For the reasons set forth below, this rejection is respectfully requested.

As mentioned above, independent claim 15 requires at least that parasitic information generated for an interconnect configuration be stored in an accessible format. The Examiner asserts that this limitation/feature is disclosed in column 4, lines 21-27 of Yip. However, the reference to writing information in an accessible format refers to

information relating to a physical layout, or interconnect configuration/shapes, of a semiconductor package (Yip, column 4, lines 20-27), not parasitic information as required by independent claim 15 of the present application. The stored description of the semiconductor package in Yip is used to determine interconnect lengths and proximity of one interconnect to another. Yip, column 4, lines 27 – 29. Contrastingly, the information stored in an accessible format as claimed in claim 15 of the present application refers to parasitic (e.g., resistance and capacitance) information generated for a particular interconnect configuration. Thus, Yip fails to disclose every limitation of claim 15. Moreover, Yip altogether discloses modeling a semiconductor package so as to reduce calculation time for mutual inductance whereas the claimed invention relates to creating an accurate wire load model.

In view of the above, Yip fails to show or suggest the present invention as recited in independent claim 15. Thus, the claim 15 is patentable over Yip. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

U.S. Patent No. 6,175,947

Claims 1-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,175,947 issued to Ponnappalli et al. (hereinafter “Ponnappalli”). For the reasons set forth below, this rejection is respectfully requested.

Independent claim 1 requires that a method for creating a wire load model comprise at least storing parasitic information in an accessible format. The Examiner asserts that this limitation/feature is disclosed in column 6, lines 26-31 of Ponnappalli.

However, the parasitic information referred to in Ponnappalli is forwarded to a module that stores *connectivity information* (i.e., which pattern belongs to which wire, which wire belongs to which net, etc.), not the parasitic information. Ponnappalli, column 6, lines 26 – 31. In other words, in Ponnappalli, although the parasitic information is used in conjunction with the stored connectivity information, the parasitic information itself is not stored in an accessible format as is required by independent claim 1 of the present application. Independent claims 6, 11, 15, and 19 also require the storing, or means for storing, parasitic information in an accessible format. Thus, Ponnappalli fails to disclose every limitation of these claims.

In view of the above, Ponnappalli fails to show or suggest the present invention as recited in claims 1, 6, 11, 15, and 19. Thus, claims 1, 6, 11, 15, and 19 are patentable over Ponnappalli. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

U.S. Patent No. 6,291,254

Claims 1-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,291,254 issued to Chou et al. (hereinafter “Chou”). For the reasons set forth below, this rejection is respectfully requested.

Independent claim 1 requires that a method for creating a wire load model comprise at least running a curve-fitting engine to create the wire load model dependent on generated parasitic information. The Examiner asserts that this limitation/feature is disclosed in column 9, lines 14 – 16 and in column 10, lines 33 – 37 of Chou. However, neither achieving convergence (as disclosed in column 9, lines 14 – 16 of Chou) nor

extrapolating an electrical property of interest (as disclosed in column 10, lines 33 – 37 of Chou) is analogous to a curve-fitting engine. As described in paragraphs [0024] – [0026] of the present application, curve-fitting is performed on parasitic information to create a wire load model. In one exemplary technique of the present invention, Equations (1) – (4) in paragraph [0024] of the present application are used to determine a load model dependent on generated parasitic information. Thus, Chou fails to disclose every limitation of these claims. Moreover, Chou is wholly directed to methods for determining interconnect process information whereas the claimed invention relates to creating a wire load model. Independent claims 6, 11, 15, and 19 also require the running of a curve-fitting engine to create a wire load model.


In view of the above, Chou fails to show or suggest the present invention as recited in claims 1, 6, 11, 15, and 19. Thus, claims 1, 6, 11, 15, and 19 are patentable over Chou. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

Applicant believes this reply to be fully responsive to all outstanding issues and place this application in condition for allowance. If this belief is incorrect, or other issues arise, do not hesitate to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.102001;P5991).

Respectfully submitted,

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